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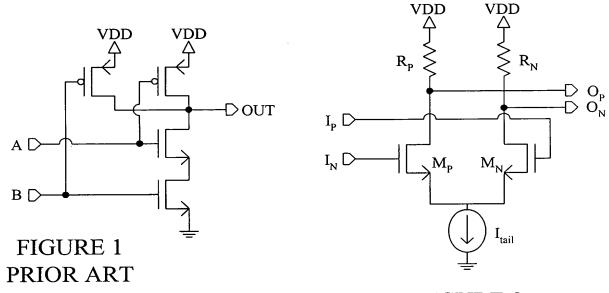


FIGURE 2 PRIOR ART

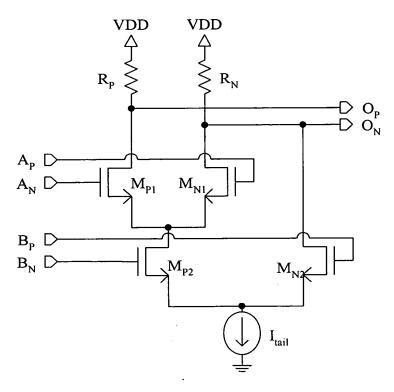


FIGURE 3 PRIOR ART

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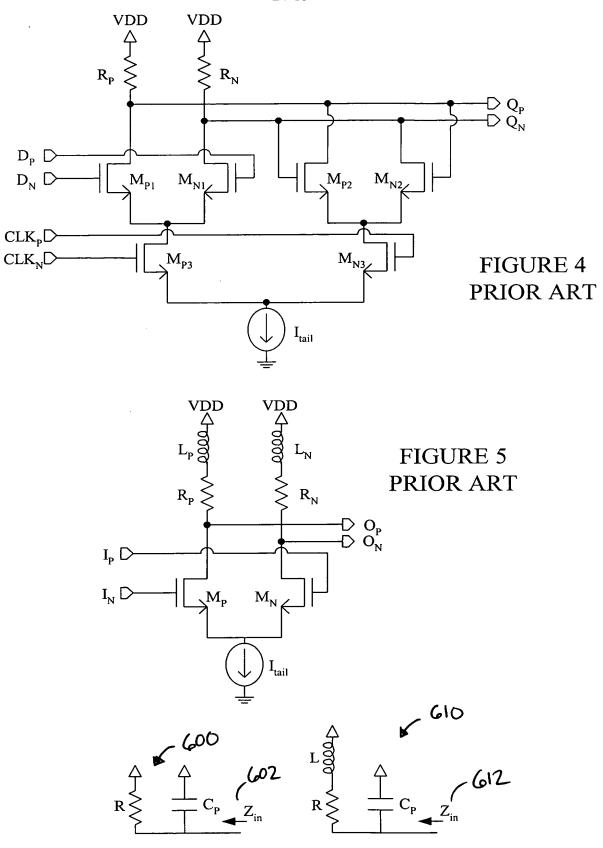


FIGURE 6

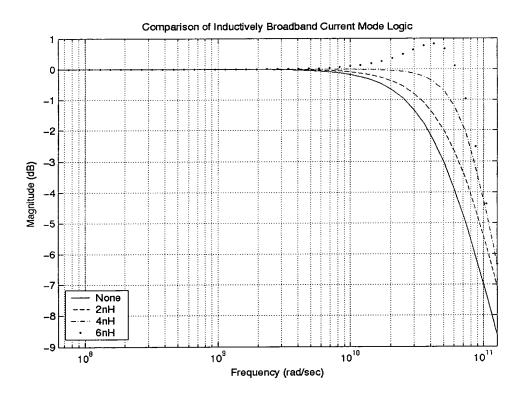


FIGURE 7

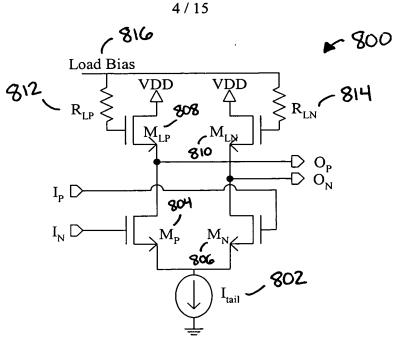
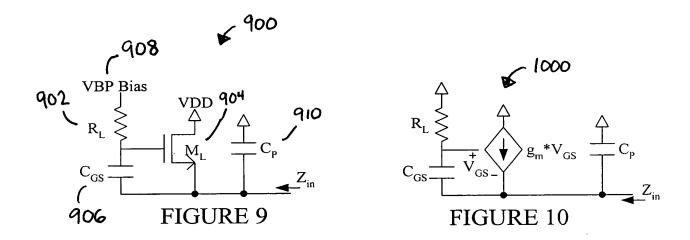


FIGURE 8



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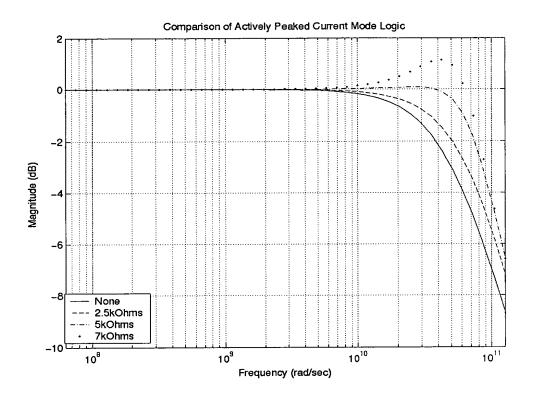


FIGURE 11

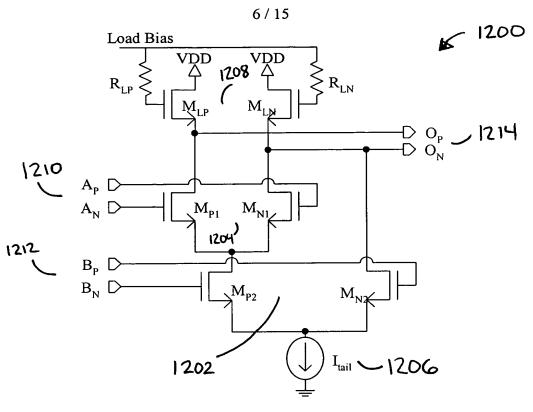


FIGURE 12

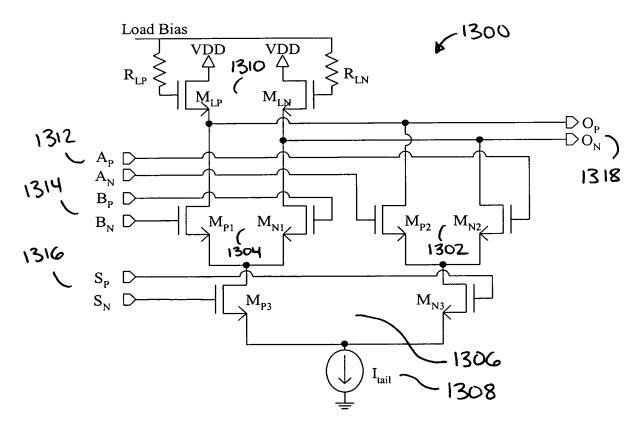
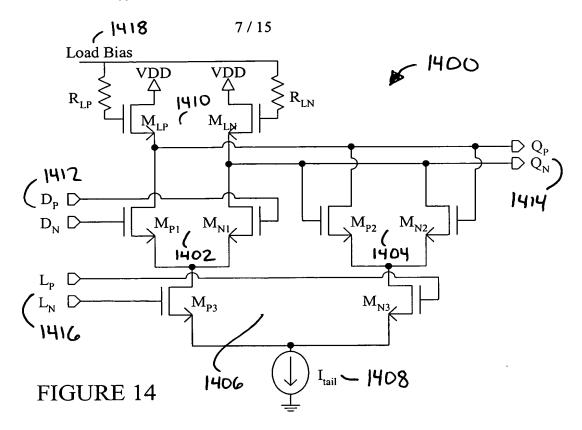
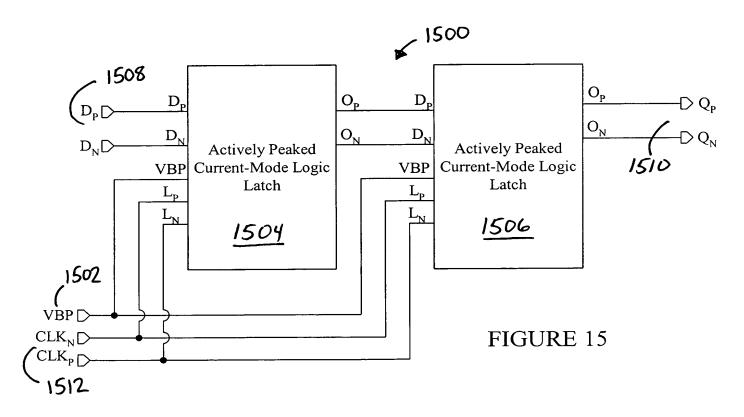


FIGURE 13





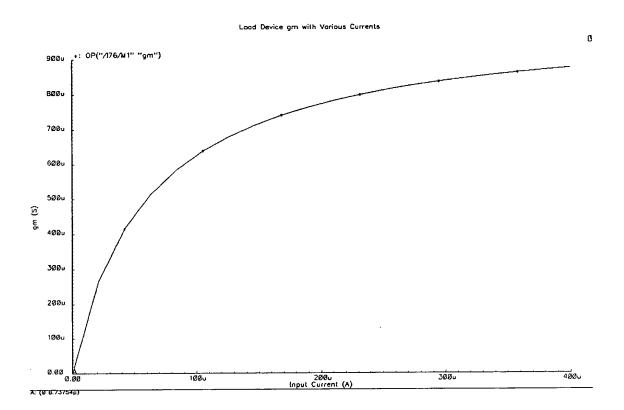
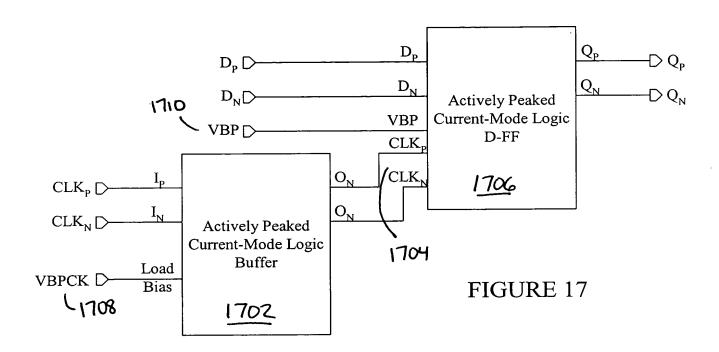


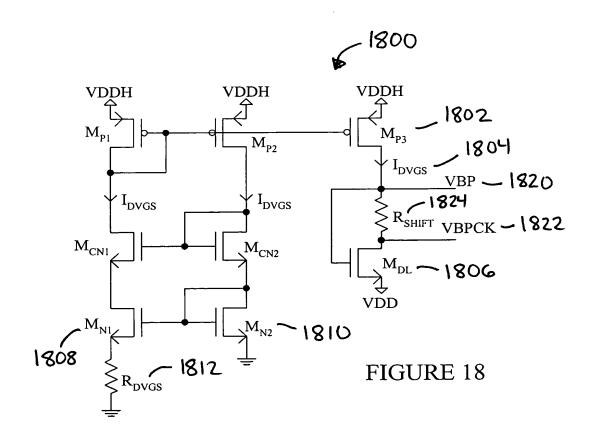
FIGURE 16

SYSTEMS AND METHODS FOR ACTIVELY PEAKED CURRENT-MODE LOGIC

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SYSTEMS AND METHODS FOR ACTIVELY PEAKED CURRENT-MODE LOGIC

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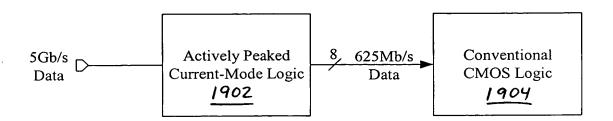


FIGURE 19

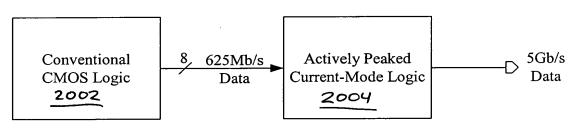


FIGURE 20

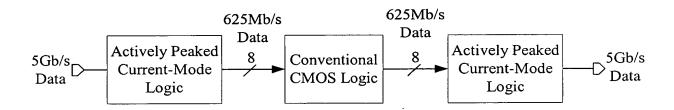
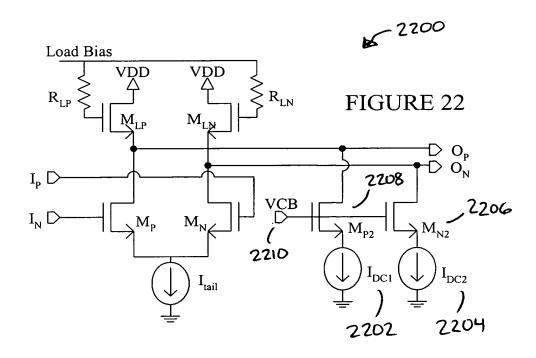
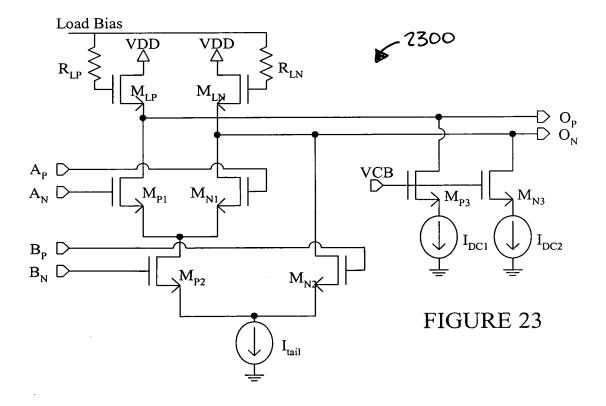


FIGURE 21

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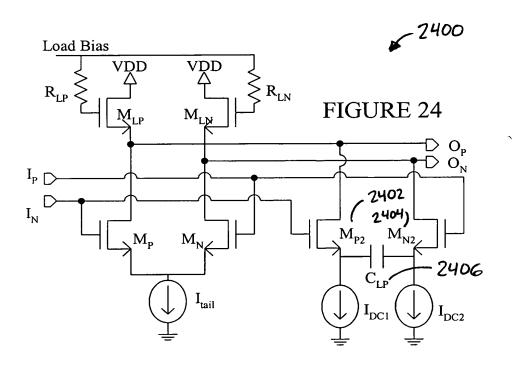


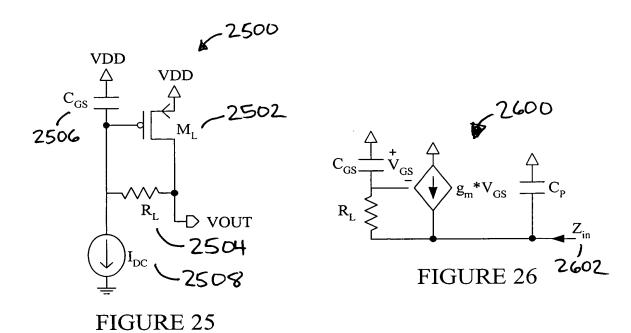


SYSTEMS AND METHODS FOR ACTIVELY PEAKED CURRENT-MODE LOGIC

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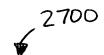
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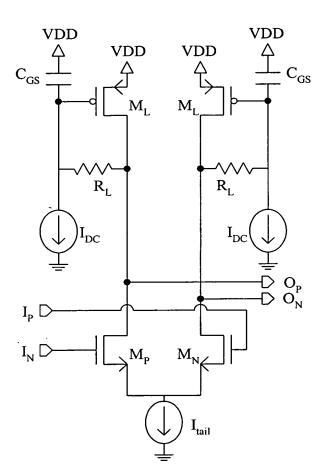


FIGURE 27

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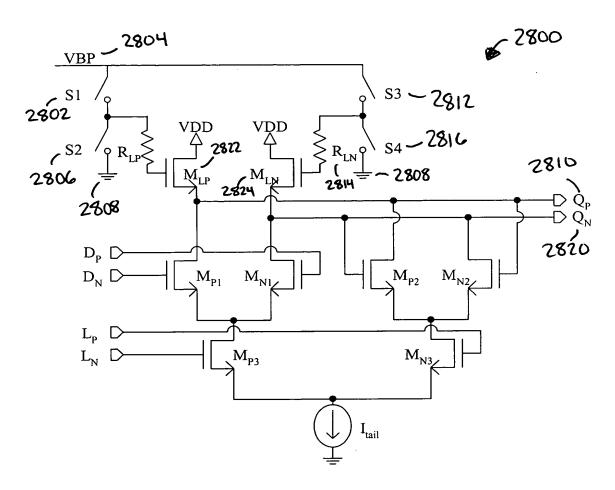
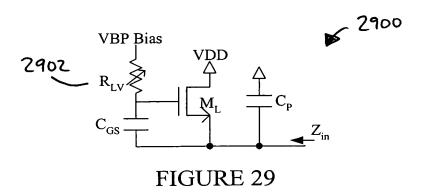


FIGURE 28



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